Comparative Analysis of Hardware Accelerated Cognitive Networks

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ABSTRACT

Wireless digital communication systems have long faced the problem of optimum bandwidth utilization in multi-user environments. Cognitive radio networks aim at addressing this problem through intelligent, flexible radio systems. Such adaptable radio systems should resolve tradeoffs between user demanded quality of service (QoS) and spectrum conditions. In the past, the cognitive radio systems implemented most of the signal processing and networking protocols in software. Such solutions relay on general purpose processors to implement changing communication schemes at a cost of reduced throughput, increased delays, and lack of guarantee of minimum QoS. On the other hand, many dedicated systems implement communication schemes in hardware using one-time-programmable chips. Recent works consider a dynamic environment where certain functions and schemes can be either implemented in hardware on FPGA or in software depending on required network performance and available hardware resources. This work investigates the design challenges of blending hardware and software in an efficient manner across two different hierarchical levels of design.